Integrated chip package structure using silicon substrate and method of manufacturing the same

Appl. No.	:	10/755,042	Confirmation No. 8665
Applicant	:	Mou-Shiung Lin, Jin-Yuan Lee, Ching-Cheng Huang	
Filed	:	January 9, 2004	
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Examiner	:	Jackson JR, Jerome	
Docket No.	:	MEGP0004USA1	
Customer No.	:	27765	

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

RESPONSE TO NON-FINAL OFFICE ACTION

Sir:

In response to the Office action of July 13, 2007, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 10 of this paper.